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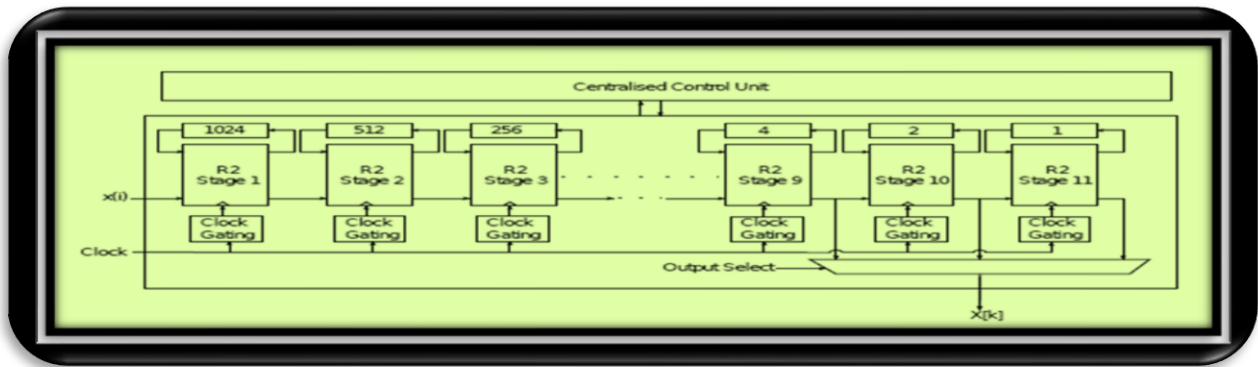
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## IEEE PROJECTS IN VLSI : 2014 – 2015

### VLC 3001. A RECONFIGURABLE FFT ARCHITECTURE FOR VARIABLE-LENGTH AND MULTI-STREAMING OFDM STANDARDS.

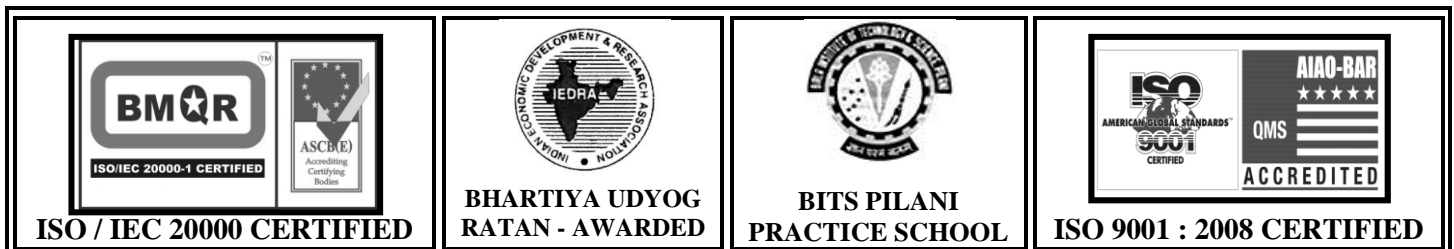
#### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** From the **EXISTING WORKS** it can be observed that most of the architectures in the literature only support either variable length or multi streaming, but not both of them simultaneously. In the **PROPOSED DESIGN** the architecture consists of a modified radix-2 single delay feedback (SDF) FFT. Experimental results show that the architecture achieves the throughput that is required by the WiMax standard and the design has additional features compared to the previous approaches. In the **MODIFICATION** we include the clock gating technique.

**DOMAIN :** LOW POWER communication.

**IEEE REFERENCE :** IEEE PAPER on Circuits and Systems,2014





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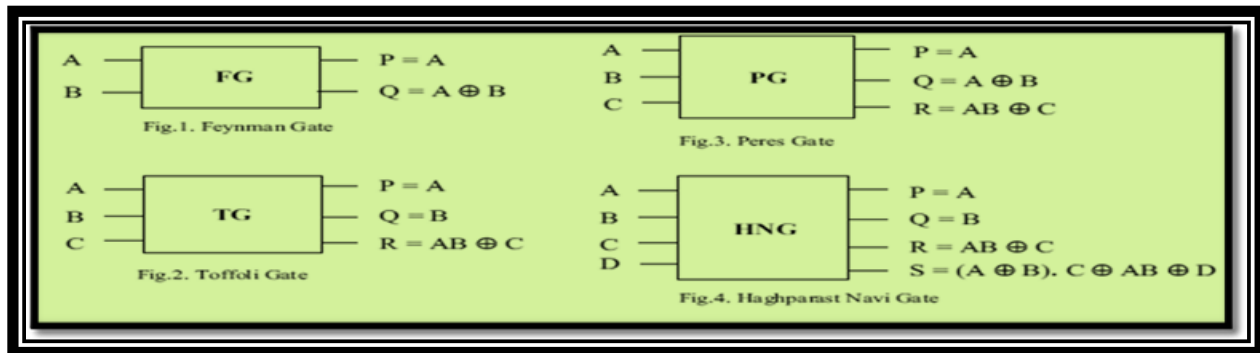
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## VLC 3002. ASIC DESIGN OF REVERSIBLE MULTIPLIER CIRCUIT

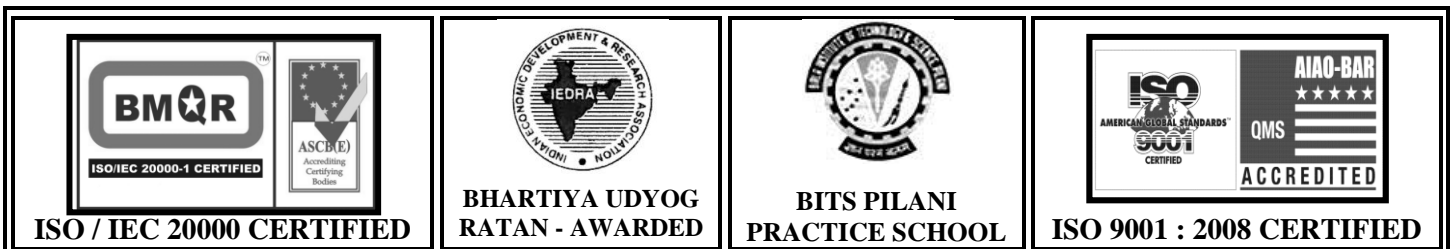
### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** In the **EXISTING DESIGN**, we have proposed Wallace reversible signed multiplier circuit by Toffoli gate Peres gate and Haghparast-Navi gate. Reversible logic is very much in demand for the future computing technologies as they are known to produce low power dissipation having its applications in Low Power CMOS, Quantum Computing, Nanotechnology, and Optical Computing. In the **PROPOSED DESIGN**, we have presented and implemented reversible Wallace signed multiplier circuit in ASIC through modified Baugh-Wooley approach. It is proved that the proposed multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, constant inputs, garbage outputs, hardware complexity, and number of transistors required. In the **MODIFICATION**, we include CSaA technique.

**DOMAIN : LOW POWER (using VEDIC MATHEMATICS).**

**IEEE REFERENCE : IEEE PAPER** on Electronic Systems, Signal Processing and Computing Technologies,2014.





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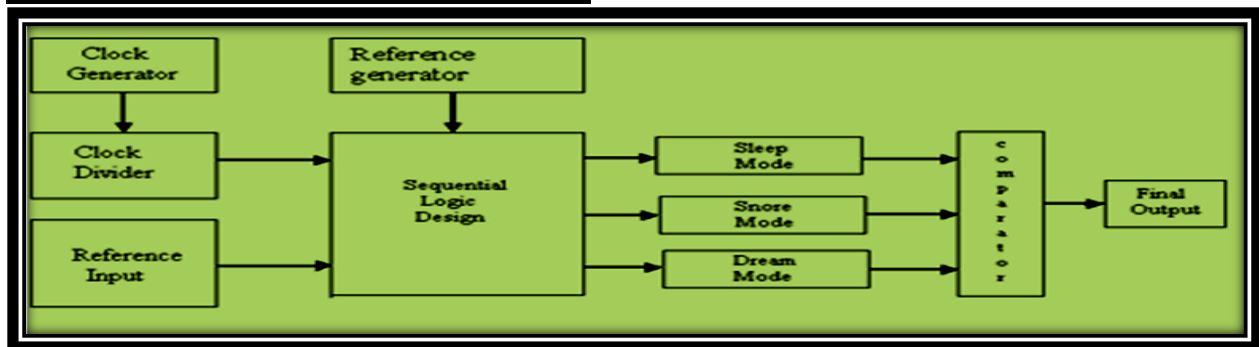
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**VLC 3003. STATIC POWER REDUCTION USING VARIATION-TOLERANT AND RECONFIGURABLE MULTI-MODE POWER SWITCH.**



**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** In the **EXISTING SYSTEM** a new power-gating technique that is tolerant to process variations and scalable to more than two intermediate power-off modes. In the Proposed design requires less design effort and offers greater power reduction and smaller area cost than the previous method. In the **PROPOSED DESIGN** to further reduce the dynamic power, systems-on-chip (SoCs) are partitioned into voltage islands with separate supply rail and unique power characteristics. Separate power management policies can be applied in each region, thereby further reducing dynamic power. In the **MODIFICATION** we combine a power gating method and clock gating method to achieve low power.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE : IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems,2014.**

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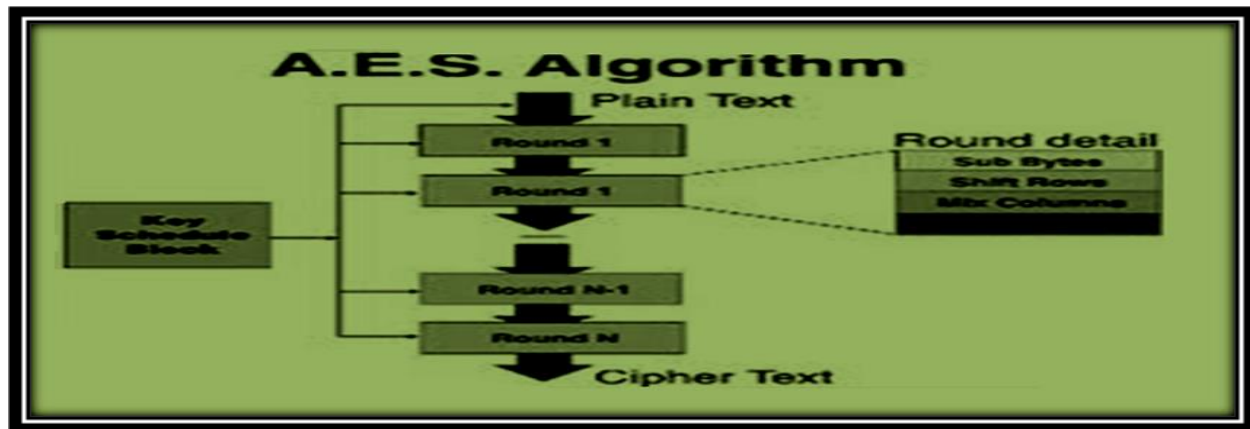
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## VLC 3004. A LOW COST RELIABLE ARCHITECTURE FOR S-BOXES IN AES PROCESSOR

### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** In the **EXISTING DESIGN**, we propose a simple architecture for AES processor. In the **PROPOSED DESIGN**, we propose a reliable architecture that allows to mask all single and permanent faults. We particularly focus on the enhancement of S-Boxes that occupy three fourths of area in AES processor. The proposed hybrid architecture exploits the inherent redundancy of AES processor's parallel implementation and embeds the redundancy in time and space. In the **MODIFICATION**, we include pipe line concept to increase the speed of the process.

**DOMAIN : CRYPTOGRAPHY.**

**IEEE REFERENCE : IEEE PAPER** on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT),2014.



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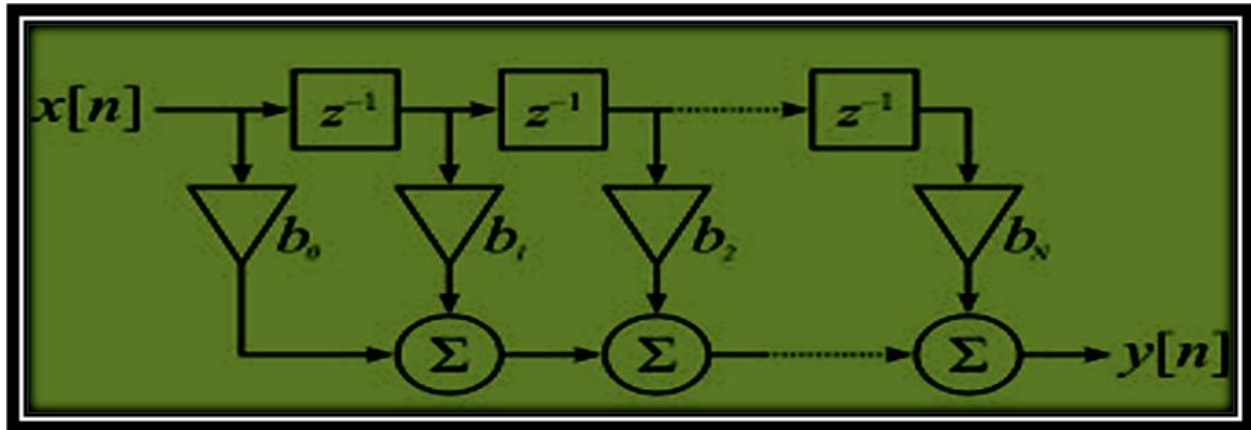
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## VLC 3005. DESIGNING HARDWARE-EFFICIENT FIXED-POINT FIR FILTERS IN AN EXPANDING SUB EXPRESSION SPACE

### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** In the **EXISTING DESIGN**, solving an LP problem is time-consuming. The **PROPOSED METHOD** takes both the filter's magnitude response and its hardware cost into consideration in the design process. The method constructs a basis set based on the fixed-point coefficients that have been synthesized already. The method employs some strategies to speed up the design process. Applying the proposed method to design twenty benchmark cases, we can obtain hardware-efficient results in a reasonable design time. In the **MODIFICATION**, we include WTM concept.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE : IEEE TRANSACTIONS** on Circuits and Systems, 2014



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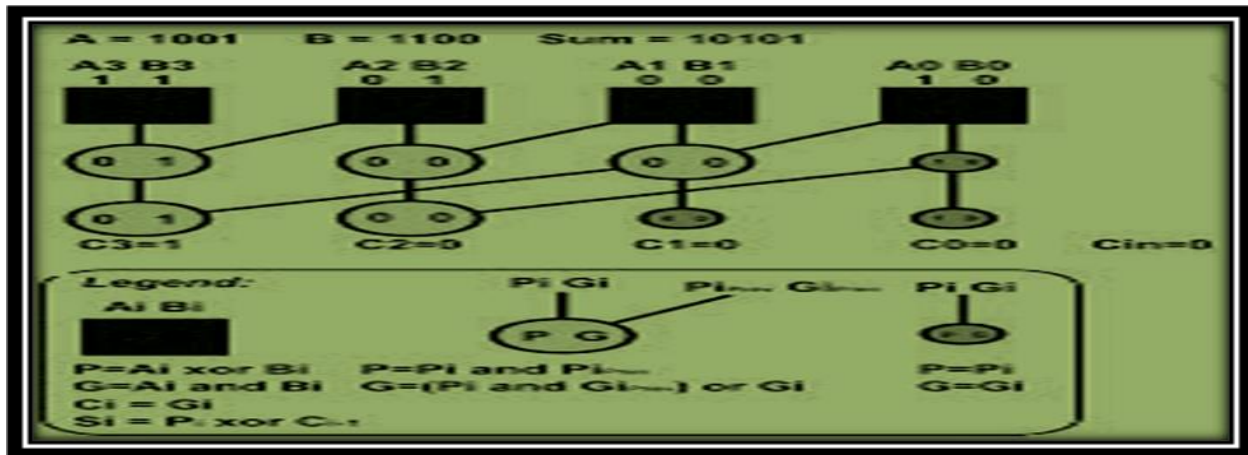
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**VLC 3006. DESIGN AND ESTIMATION OF DELAY, POWER  
AND AREA FOR PARALLEL PREFIX ADDERS**

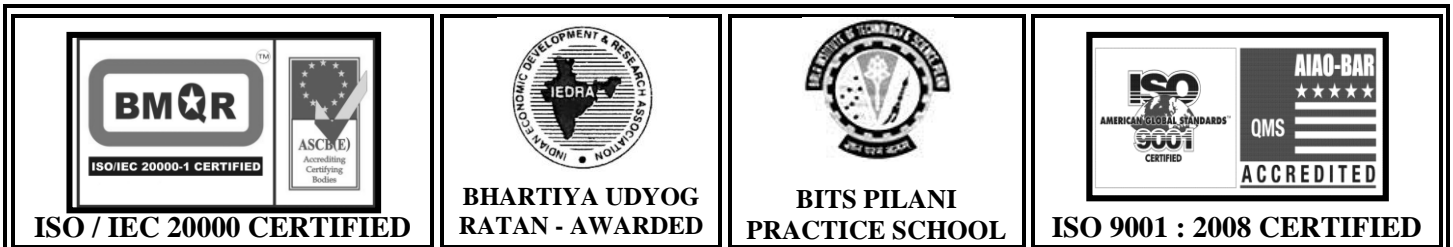
**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** In Very Large Scale Integration (VLSI) designs, Parallel prefix adders (PPA) have the better delay performance. In the **PROPOSED DESIGN**, we investigate four types of PPA's (Kogge Stone Adder (KSA), Spanning Tree Adder (STA), Brent Kung Adder (BKA) and Sparse Kogge Stone Adder (SKA)). Additionally Ripple Carry Adder (RCA), Carry Lookahead Adder (CLA) and Carry Skip Adder (CSA) are also investigated. In the **MODIFICATION** we include the pipe line concept.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE : IEEE PAPER** on Very Large Scale Integration (VLSI) systems, 2014.





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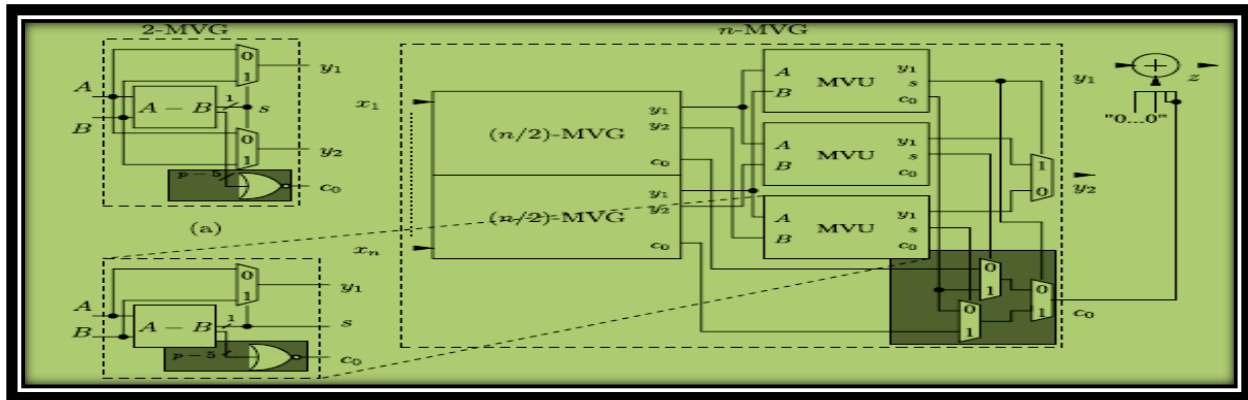
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**VLC 3007. SIMPLIFIED LOG-MAP ALGORITHM FOR VERY LOW-COMPLEXITY TURBO DECODER HARDWARE ARCHITECTURES**

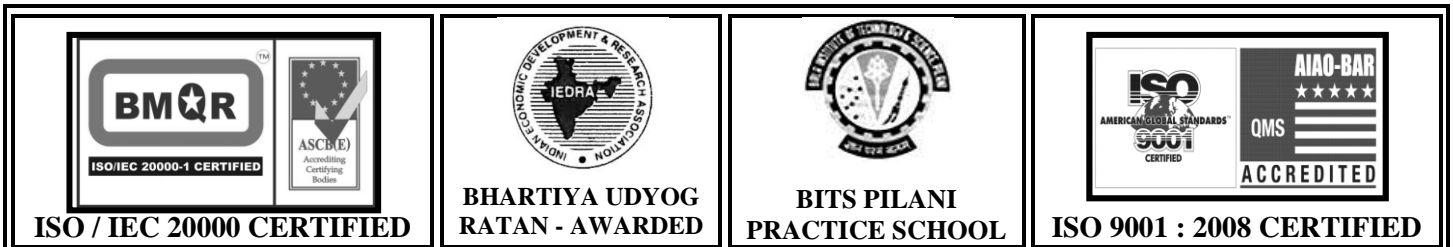
**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** In the **EXISTING DESIGN**, we propose the constant logarithmic-maximum a posteriori (Log-MAP). In the **PROPOSED DESIGN**, we implemented the n-input max approximation algorithm is performed. In the **MODIFICATION** the LUT log BCJR is designed with Clock gating technique which leads to reduction in Power consumption and energy consumption reduction is carried out. The circuit is converted into digital hardware.

**DOMAIN : CRYPTOGRAPHY**

**IEEE REFERENCE : IEEE TRANSACTIONS on Instrumentation and Measurement, 2014**





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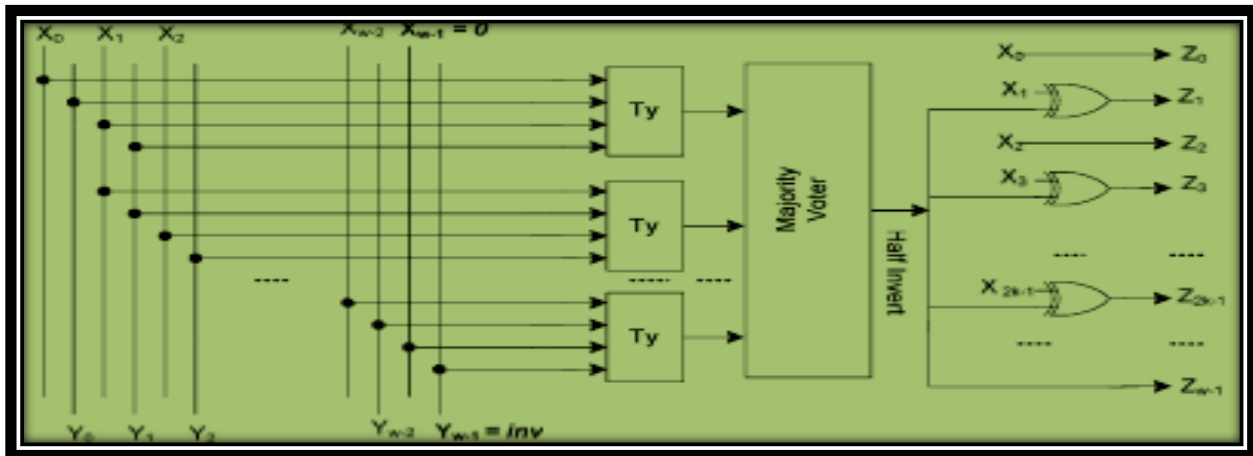
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**VLC 3008. DATA ENCODING TECHNIQUES FOR REDUCING ENERGY CONSUMPTION IN NETWORK-ON-CHIP**



**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** This paper concept depend on traffic flow in the chip. In the **EXISTING DESIGN** not suitable for dynamic NOC. In the **PROPOSED DESIGN**, we propose a set of data encoding schemes aimed at reducing the power dissipated by the links of an NoC. Experiments carried out on both synthetic and real traffic scenarios show the effectiveness of the proposed schemes. In the **MODIFICATION** we design a simple traffic flow concept.

**DOMAIN :** Network on chip.

**IEEE REFERENCE :** IEEE TRANSACTIONS on very large scale integration (VLSI) systems,2014

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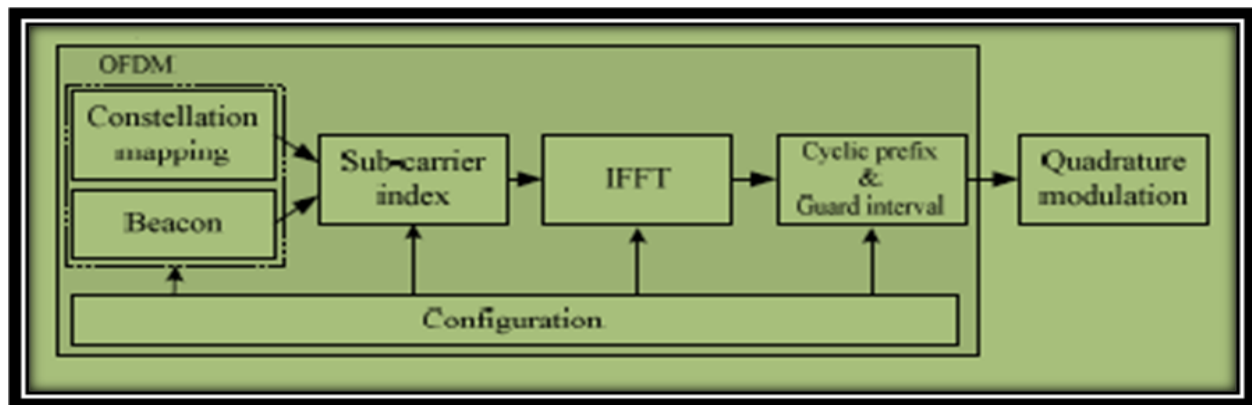
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## VLC 3009. A NOVEL RECONFIGURABLE ARCHITECTURE FOR GENERIC OFDM MODULATOR BASED ON FPGA

### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** The **EXISTING DESIGN**, only for specific communication standards. In the **PROPOSED DESIGN**, to implement OFDM modulator through a novel reconfigurable architecture to meet different communication standards. This work divides the design into five main functional subsystems: constellation mapping, beacon adding, sub-carrier index, IFFT, cyclic prefix and guard interval adding and configuration. In the **MODIFICATION** we include any one of the low power related concept

**DOMAIN:** **LOW POWER communication.**

**IEEE REFERENCE:** **IEEE PAPER** on Advanced Communication Technology, 2014



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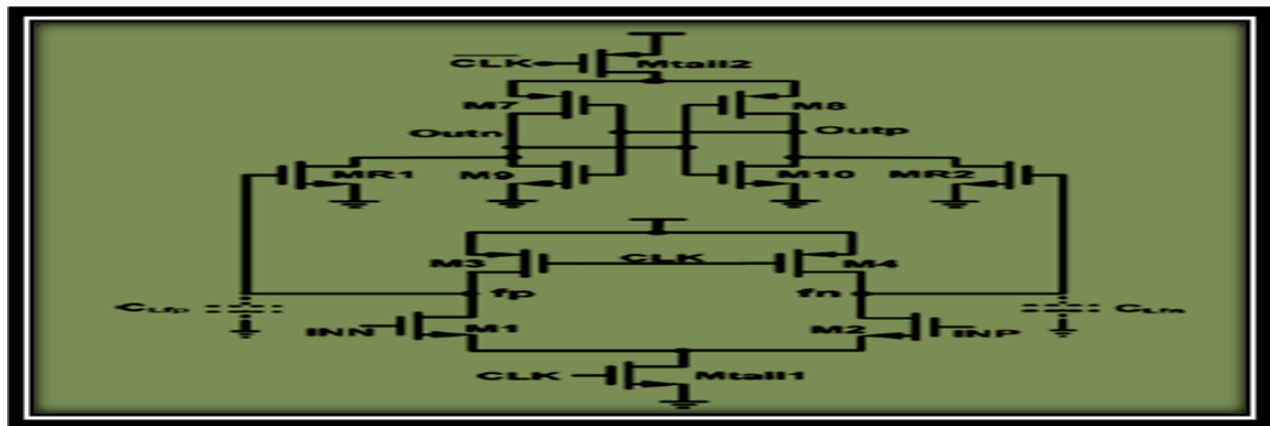
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## VLC 4010. ANALYSIS AND DESIGN OF A LOW-VOLTAGE LOW-POWER DOUBLE-TAIL COMPARATOR

### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** In the **EXISTING DESIGN** the designed comparator was take high power. In the **PROPOSED DESIGN** dynamic comparator is constructed, where the circuit of a conventional double tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. In the **MODIFICATION** a this design is implemented with different **cmos** technology.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE : IEEE TRANSACTIONS** on very large scale integration (VLSI) systems,2014.



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## VLC 4011. ANALYSIS OF IMAGE COMPRESSION ALGORITHM USING DCT AND DWT TRANSFORMS

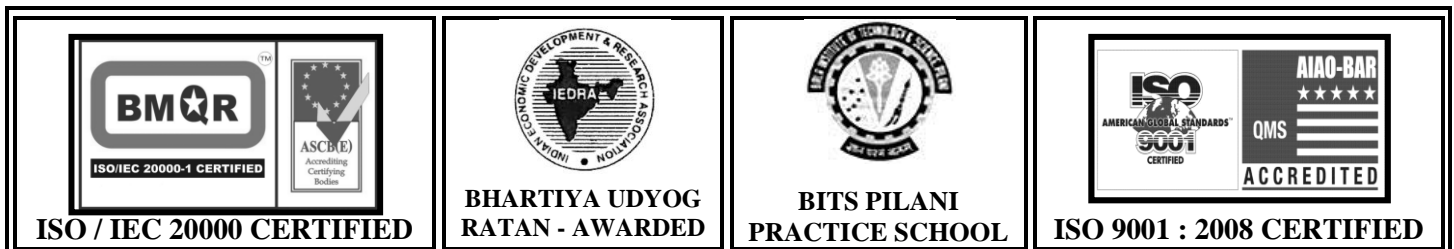
### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** The **PROPOSED DESIGN** is a flexible hardware architecture of multi-level decomposition Discrete Wavelet Transform (DWT) for image compression applications to eliminate redundant information from the transmitted images or video frames over the wireless channel. It facilitates to images of size  $64 \times 64$ ,  $128 \times 128$ ,  $256 \times 256$ , and  $512 \times 512$  pixels and capable of seven levels of decomposition. In order to reduce computational complexities, Fast Haar Wavelet Transform (FHWT) is used. The reduction in the resource usage of this 2D DWT multilevel FPGA core can be used to counter severe hardware constraints of various wireless and mobile device applications. In the **MODIFIVATION** we perform the process for **PSNR** ratio improvement.

**DOMAIN : IMAGE PROCESSING.**

**IEEE REFERENCE : IEEE PAPER** on Computer Science and Software Engineering, 2014.





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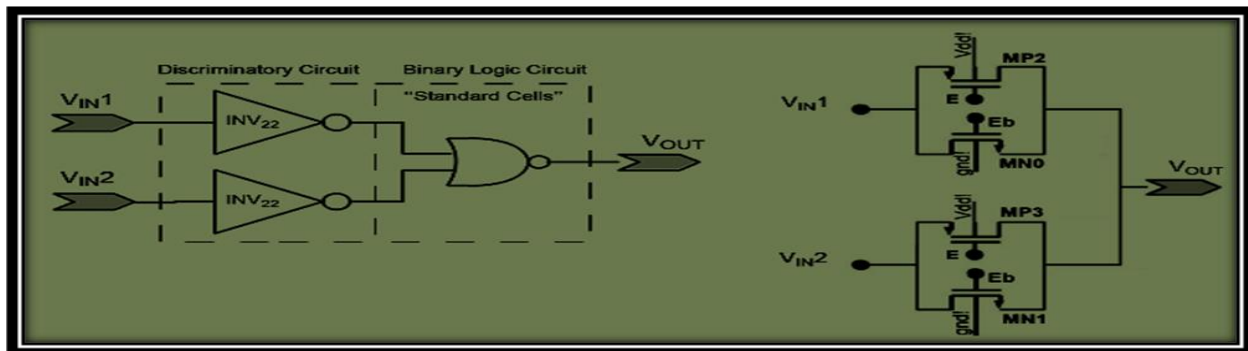
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## VLC 3012. UNIVERSAL SET OF CMOS GATES FOR THE SYNTHESIS OF MULTIPLE VALUED LOGIC DIGITAL CIRCUITS

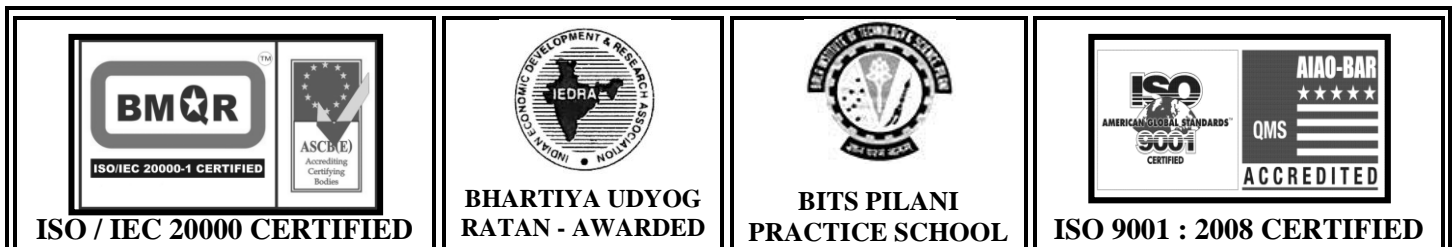
### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** This paper deals with: 1) the design and implementation of a universal set of IC gates, CMOS 0.35 $\mu$ m technology, that carry out extended AND operators: eAND1, eAND2, eAND3, Successor (SUC), and Maximum (MAX) operators to perform synthesis of any MVL digital circuits; and 2) the synthesis of an MVL multiplexer and latch memory circuits, based on the ICMVL gates, to illustrate the utilization of the proposed IC MVL gates for quaternary MVL. The PROPOSED DESIGN allow designing MVL digital circuit taking advantage of the knowledge coming from the binary circuits. By using a methodology based on the Boolean algebra, digital circuits designers can take advantage of it to decrease the design learn curve.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE: IEEE TRANSACTIONS on Circuits and Systems, 2014.**





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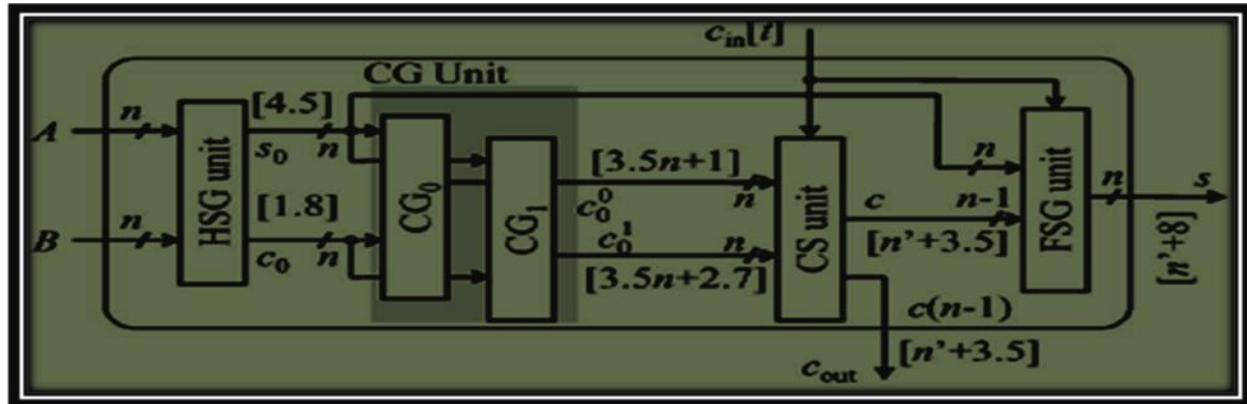
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**VLC 3013. AREA-DELAY-POWER EFFICIENT CARRY-SELECT ADDER**

**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** The redundant logic operations present in the **EXISTING DESIGN**. In the **PROPOSED DESIGN**, the carry select (CS) operation is scheduled before the calculation of final-sum, which is different from the conventional approach. Bit patterns of two anticipating carry words (corresponding to  $c_{in} = 0$  and  $1$ ) and fixed  $c_{in}$  bits are used for logic optimization of CS and generation units. An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less area and delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT) CSLA.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE:** IEEE TRANSACTIONS on Circuits and Systems,2014.

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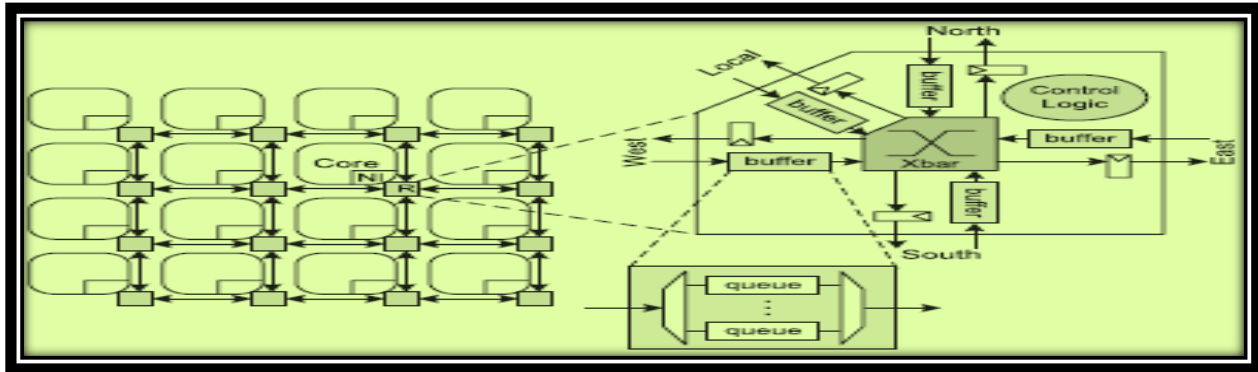
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## VLC 3014. ACHIEVING HIGH-PERFORMANCE ON-CHIP NETWORKS WITH SHARED-BUFFER ROUTERS





### ARCHITECTURE DIAGRAM:



**DESCRIPTION** : On-chip routers typically have buffers dedicated to their input or output ports for temporarily storing packets in case contention occurs on output physical channels. Buffers, unfortunately, consume significant portions of router area and power budgets. While running a traffic trace, however, not all input ports of routers have incoming packets needed to be transferred simultaneously. Therefore, a large number of buffer queues in the network are empty and other queues are mostly busy. This observation motivates us to design router architecture with shared queues (RoShaQ), router architecture that maximizes buffer utilization by allowing the sharing multiple buffer queues among input ports.

**DOMAIN** : Network on chip.

**IEEE REFERENCE** : IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) systems,2014

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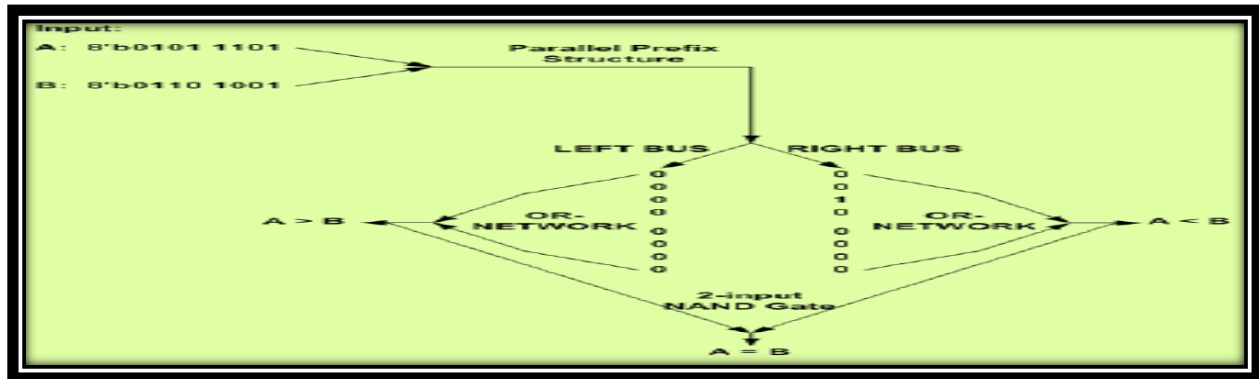
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**VLC 3015. SCALABLE DIGITAL CMOS COMPARATOR USING A PARALLEL PREFIX TREE**



**ARCHITECTURE DIAGRAM:**



**DESCRIPTION:** The **EXISTING DESIGN** doesn't have required power efficiency. In the **PROPOSED DESIGN**, we present a new comparator design featuring wide-range and high-speed operation using only conventional digital CMOS cells. Our comparator exploits a novel scalable parallel prefix structure that leverages the comparison outcome of the most significant bit, proceeding bitwise toward the least significant bit only when the compared bits are equal. This method reduces dynamic power dissipation by eliminating unnecessary transitions in a parallel prefix structure that generates the N-bit comparison result after  $\log_4 N + \log_{16} N + 4$  CMOS gate delays. The main advantages of our design are high speed and power efficiency, maintained over a wide range.

**DOMAIN : LOW POWER.**

**IEEE REFERENCE : IEEE TRANSACTIONS** on Very Large Scale Integration (VLSI) systems,2014

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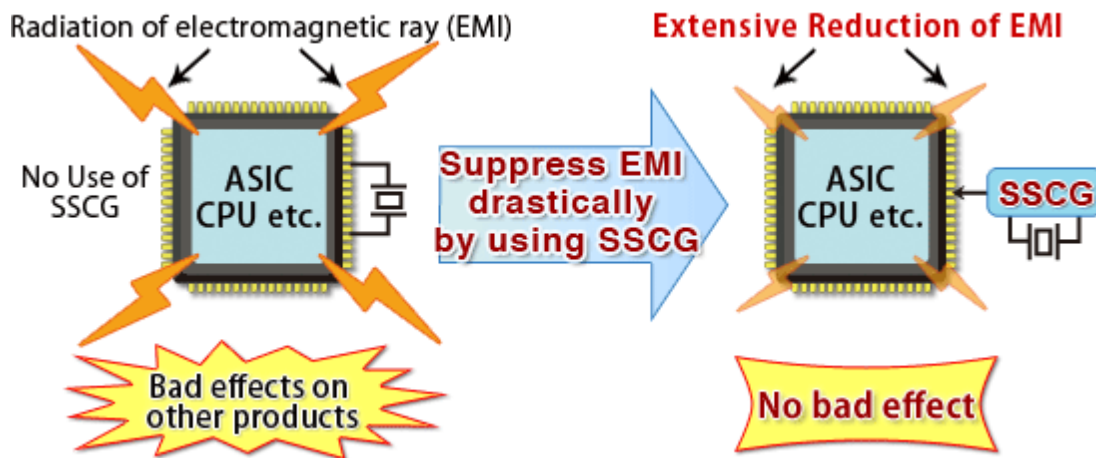
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## VLC 3016 : A LOW-COST LOW-POWER ALL-DIGITAL SPREAD-SPECTRUM CLOCK GENERATOR



### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** Electromagnetic interference (EMI) is a major challenge for designers of electronic devices. Strict guidelines enforced by the FCC and European Union regulate the amount of EMI a system can generate. Frequency references, whether crystal oscillators or silicon-based PLLs, can be a major source of EMI on circuit boards. Spread spectrum clocking is a technique where the clock frequency is modulated slightly to lower the peak energy generated by a clock. Spread spectrum clocking lowers clock-generated EMI from both the fundamental frequency and subsequent harmonics, thereby reducing the total system EMI.

**DOMAIN : SIGNAL PROCESSING.**

**IEEE REFERENCE : IEEE TRANSACTIONS ON Very Large Scale Integration (VLSI) Systems, 2014.**

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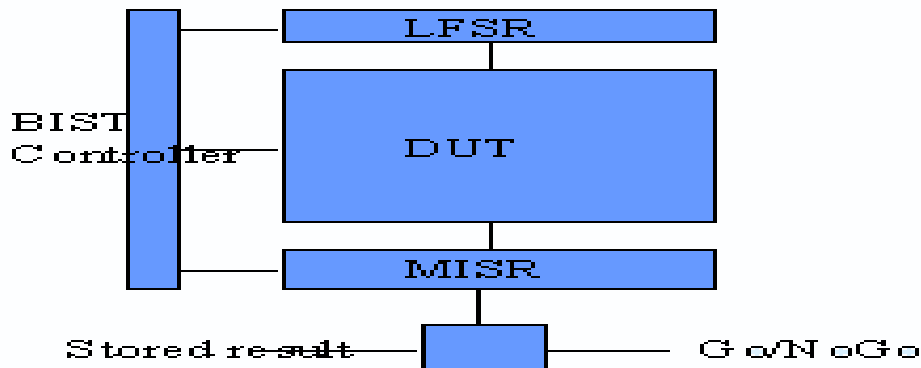
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## VLC 3017. INPUT VECTOR MONITORING CONCURRENT BIST ARCHITECTURE USING SRAM CELLS

### ARCHITECTURE DIAGRAM

## Built In Self Test



**DESCRIPTION :** Input vector monitoring concurrent BIST techniques have been proposed to avoid this performance degradation. The concurrent testing of ROM modules is presented in this project. During test mode, the inputs generated by a test generator module are applied to the inputs of the circuit under test (CUT) and the responses are captured into a response verifier (RV).

**DOMAIN:** Built in Self Test

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2014



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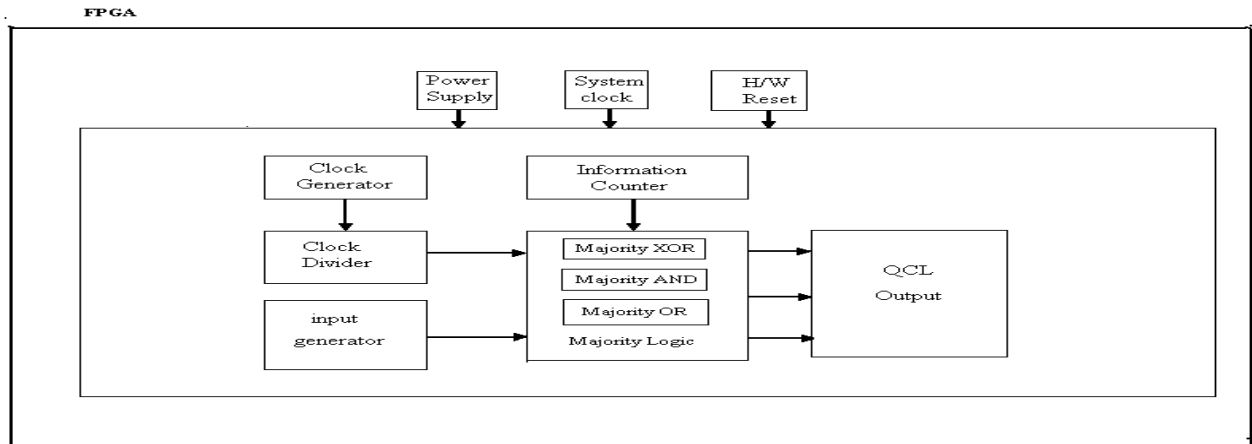
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**VLC 3018. AREA-DELAY EFFICIENT BINARY ADDERS IN QCA ARCHITECTURE DIAGRAM**



**DESCRIPTION :** The logic unit in QCA is the QCA cell which was proposed by researchers at the University of Notre Dame. The QCA cell is composed of 4 or 5 quantum dots. Before we examine the potential functionality of these cells we need to know a few basic facts about quantum dots. A quantum dot is a nanometer sized structure that is capable of trapping electrons in three dimensions. Quantum dots are made by creating an island of conductive material surrounded by insulating material. Electrons that enter the quantum dot will be confined because of the high potential required to escape.

**DOMAIN: Low Power.**

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2014

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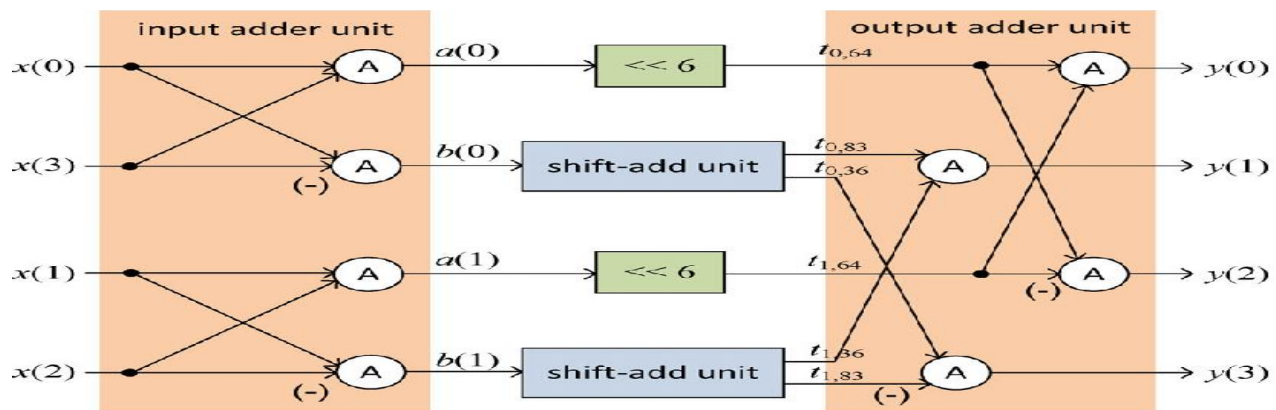
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**VLC 3019.EFFICIENT INTEGER DCT ARCHITECTURES FOR HEVC**





**ARCHITECTURE DIAGRAM**



**DESCRIPTION:** The discrete cosine transform (DCT) plays a vital role in video compression due to its near-optimal decorrelation efficiency. We have designed scalable and reusable architectures for 1-D and 2-D integer DCTs for HEVC that could be reused for any of the prescribed lengths with the same throughput of processing irrespective of transform size.

**DOMAIN: Image Processing.**

**IEEE REFERENCE : IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems,2014**

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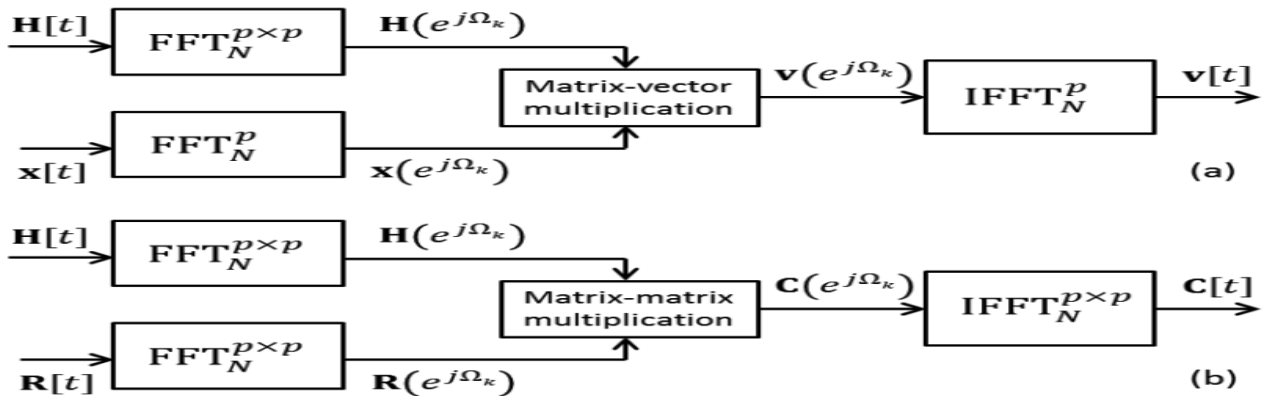
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**VLC 3020. NOVEL RECONFIGURABLE HARDWARE ARCHITECTURE FOR POLYNOMIAL MATRIX MULTIPLICATIONS**

**ARCHITECTURE DIAGRAM**



**DESCRIPTION:** The proposed architecture gives low execution times while utilizing limited FPGA resources. It yields a good approximation to the polynomial matrix computation provided by its double-precision counterpart running in MATLAB for both real- and complex-valued data. The architecture has been developed using the Xilinx system generator for DSP tool which offers a visual interface and a number of standard modules for speedy design.

**DOMAIN: Low Power**

**IEEE REFERENCE : IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2014**

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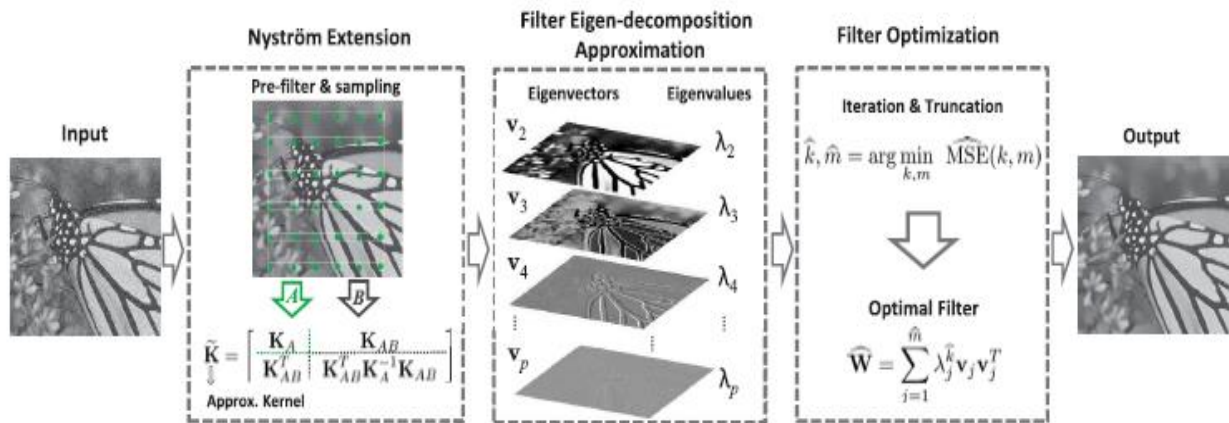
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**VLC 3021. GLOBAL IMAGE DENOISING**

**ARCHITECTURE DIAGRAM**



**DESCRIPTION:** The block diagram of the proposed global image denoising (GLIDE) framework is illustrated in above diagram. As can be seen, after applying a pre-filter on the noisy image, a small fraction of the pixels are sampled to be fed to the Nystrom method. Then, the global filter is approximated through its eigenvalues and eigenvectors. The final estimate of the image is constructed by means of shrinkage of the filter eigenvalues.

**DOMAIN: Image Processing.**

**IEEE REFERENCE : IEEE TRANSACTIONS on Image Processing,2014**

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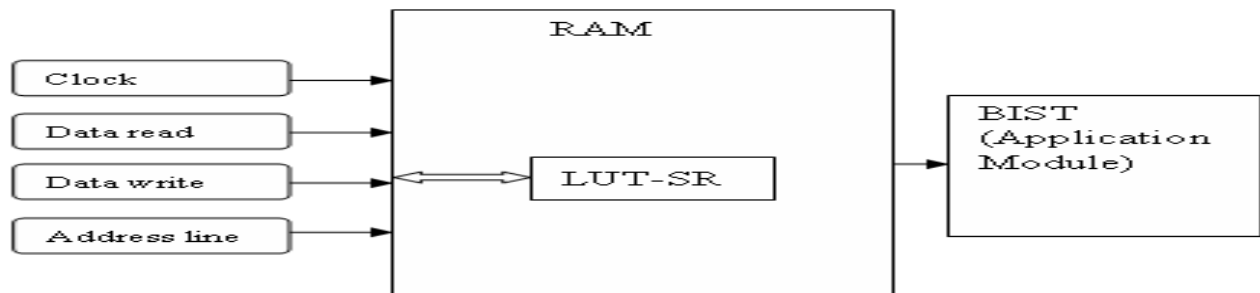
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## VLC 3022. THE LUT-SR FAMILY OF UNIFORM RANDOM NUMBER GENERATORS FOR FPGA ARCHITECTURES

### ARCHITECTURE DIAGRAM:



**DESCRIPTION:** The **EXISTING SYSTEM**, describes a type of FPGA RNG called a LUT-FIFO.LUT using FIFO is to decrease the speed of operation. The **PROPOSED SYSTEM**, describes a type of FPGA RNG called a LUT-SR RNG, which takes advantage of bitwise XOR operations and the ability to turn lookup tables (LUTs) into shift registers of varying lengths. The LUT-SR generators can also be expressed using a simple C++ algorithm contained within this existing design. Our **MODIFICATION**, is the LUT Random number generator is designed using Pseudo random codes generator which is high speed generator with different frequency ranging is realized here.

**DOMAIN:** Memory Design

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems,2013



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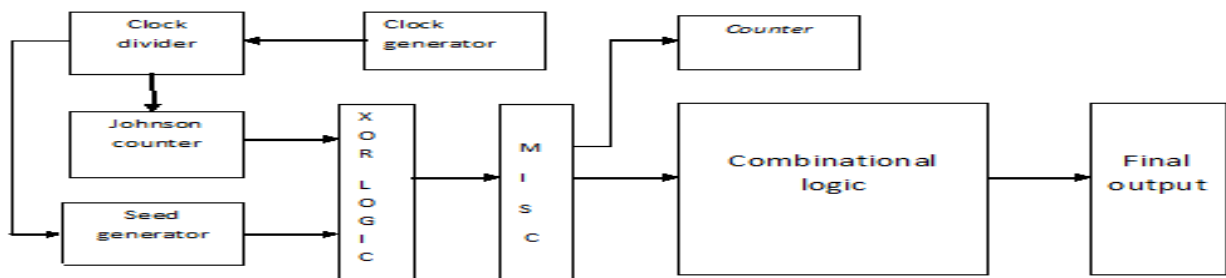
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## VLC 3023. TEST PATTERNS OF MULTIPLE SIC VECTORS: THEORY AND APPLICATION IN BIST SCHEMES

### ARCHITECTURE DIAGRAM



**DESCRIPTION :** In the **EXISTING SYSTEM**, there is no test pattern generator for bist. In the **PROPOSED SYSTEM**, a Test Pattern Generator is flexible to both the test-per-clock and the test-per-scan schemes were realized. A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced MSIC sequences have the favorable features of uniform distribution and low input transition density. The performances of the designed TPGs and the circuits under test with 45 nm are evaluated. In the **MODIFICATION**, part a sample module is created to do the Built in self test algorithm using automatic test pattern generation also user defined test pattern generation option also we design, The entire hardware is realized as digital logical circuits and the test results are simulated in Modelsim.

**DOMAIN: Built in Self Test**

**IEEE REFERENCE : IEEE TRANSACTIONS on Very Large Scale  
Integration (VLSI) Systems 2013**



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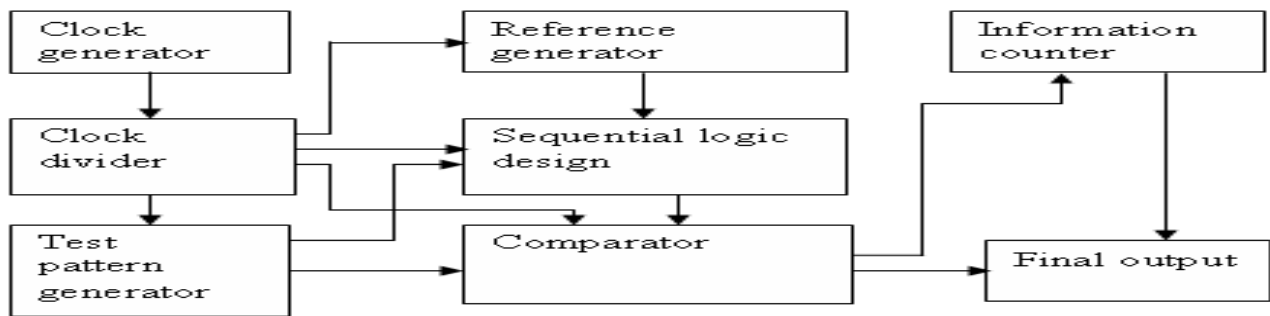
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**VLC 3024. POWER-PLANNING-AWARE SOFT ERROR HARDENING VIA SELECTIVE VOLTAGE ASSIGNMENT**



**ARCHITECTURE DIAGRAM**



**DESCRIPTION :** In the **EXISTING SYSTEM**, glitch can't be removed in the high speed system. In the **PROPOSED SYSTEM**, we designed a power-planning-aware methodology using dual supply voltages for soft error hardening. Given a constraint on power overhead, our proposed framework can minimize the soft error rate (SER) of a circuit via selective voltage assignment. In the 70-nm predictive technology model, circuit SER can be reduced by 23% on top of SER-aware gate resizing. For power-planning awareness, a bi-partitioning technique based on a simplified version of the Fiduccia-Mattheyses (FM) algorithm is presented. In the **MODIFICATION**, part we design the improved version of dual VDD SER reduction Algorithm is implemented and FM based bi positioning circuit also designed. cost function also designed as a improved version.

**DOMAIN:** Error Detection & Correction

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2013

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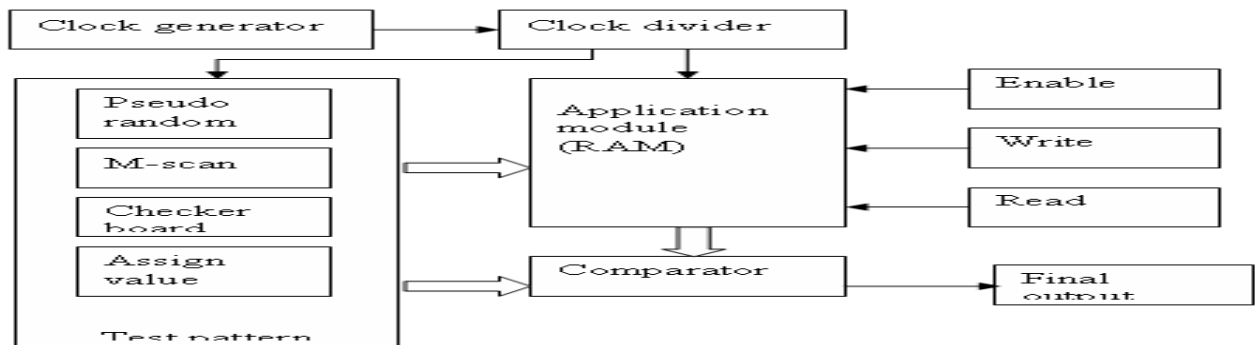
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## VLC 3025. TIME-BASED ALL-DIGITAL TECHNIQUE FOR ANALOG BUILT-IN SELF-TEST





### ARCHITECTURE DIAGRAM



**DESCRIPTION :** In the **EXISTING SYSTEM**, the bist is designed using only based power. In the **PROPOSED SYSTEM**, the built in self test is designed using distributed architecture and the clock is routed serially, the performance is measured a certain analog voltage, the corresponding subsampled signal pair is fed to a delay measurement unit to measure the skew between this pair. The accuracy is measured here. In the **MODIFICATION**, part a Built in self test is performed using a sample module which is nothing but a random access memory is designed The BIST RAM is considered under test and difference advanced test cases are given to test the circuit, The performance is measure in such a way the power consumption reduction, Area efficiency is achieved.

**DOMAIN :** Silicon Validation.

**IEEE REFERENCE :** IEEE TRANSACTIONS on very large scale integration (VLSI) systems, 2013

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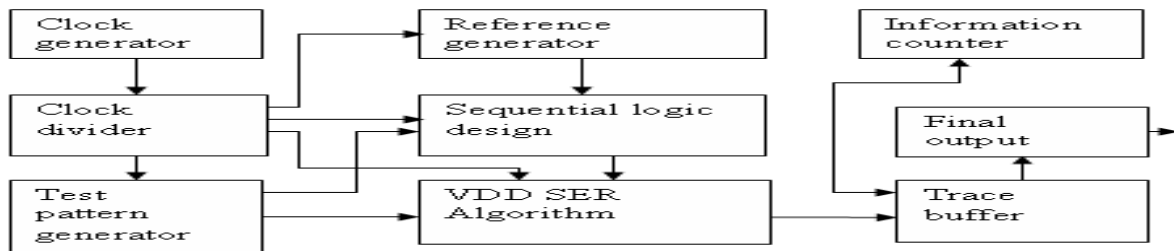
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## VLC 3026. RATS: RESTORATION-AWARE TRACE SIGNAL SELECTION FOR POST-SILICON VALIDATION

### ARCHITECTURE DIAGRAM



**DESCRIPTION :** In the **EXISTING SYSTEM**, there is no restorability concept for signal processing. In the **PROPOSED SYSTEM**, they depend on partial restorability computations that are not effective in restoring maximum signal states. They also require long signal selection time due to inefficient computation as well as operating on gate-level net list. We have proposed a signal selection approach based on total restorability at gate-level, which is computationally more efficient (10 times faster) and can restore up to three times more signals compared to previous methods. In the **MODIFICATION**, the silicon validation is done by providing various test pattern inputs to do various test sets are created to test the silicon plates, a trigger using also controlled by a control unit which perform the validation task at best level.

**DOMAIN :** Error Checking , Silicon Validation.

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems,2013



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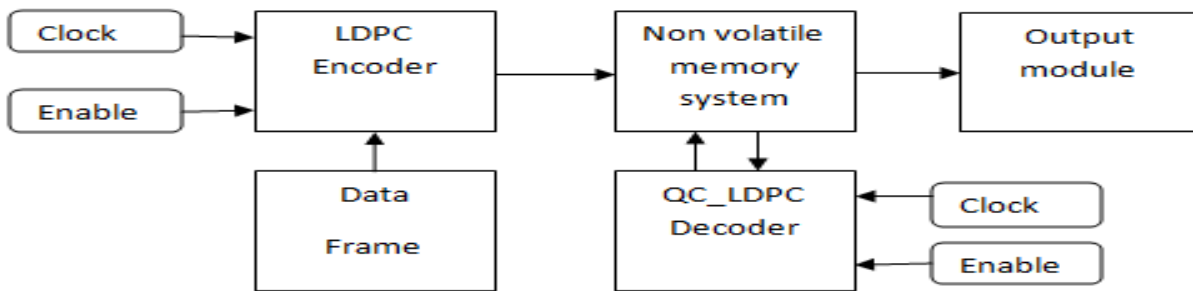
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**VLC 3027. ERROR DETECTION IN MAJORITY LOGIC DECODING OF EUCLIDEAN GEOMETRY LOW DENSITY PARITY CHECK (EG-LDPC) CODES**

**ARCHITECTURE DIAGRAM**



**DESCRIPTION :** The **EXISTING SYSTEM**, have poor error detection capability. In the **PROPOSED SYSTEM**, the Low density parity check algorithm alone implemented with the constant input data even after the first iteration being completed the second set of iteration started only when new second data has given. In the **MODIFICATION**, a Memory is designed with encoder and decoder, We proposing a system which encrypt the incoming data using LDPC encoder and stores the same in to the memory which is designed, the stored data is decrypted using Majority decoder and a comparator. Whenever a data get corrupted or lost due to transient problem using the high efficient LDPC decode algorithm we can retrieve the original information to be stored into the memory.

**DOMAIN : Cryptography**

**IEEE REFERENCE : IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems,2013**

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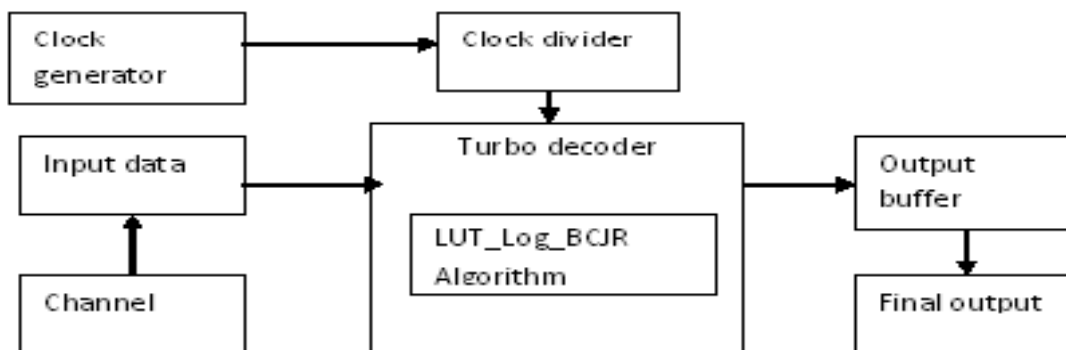
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## VLC 3028. A LOW-COMPLEXITY TURBO DECODER ARCHITECTURE FOR ENERGY-EFFICIENT WIRELESS SENSOR NETWORKS

### ARCHITECTURE DIAGRAM



**DESCRIPTION :** In the **EXISTING SYSTEM**, the speed of operation was too slow. In this **PROPOSED SYSTEM**, we implemented the LUT-Log-BCJR architecture into its most fundamental add compare select (ACS) operations and perform them using a novel low-complexity ACS unit. The demonstration also simulates the energy efficiency, and power reduction as shown in this paper. In the **MODIFICATION**, part the LUT log BCJR is designed with Clock gating technique which leads to reduction in Power consumption and energy consumption reduction is carried out. The circuit is converted into digital hardware.

**DOMAIN :** Cryptography

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2013



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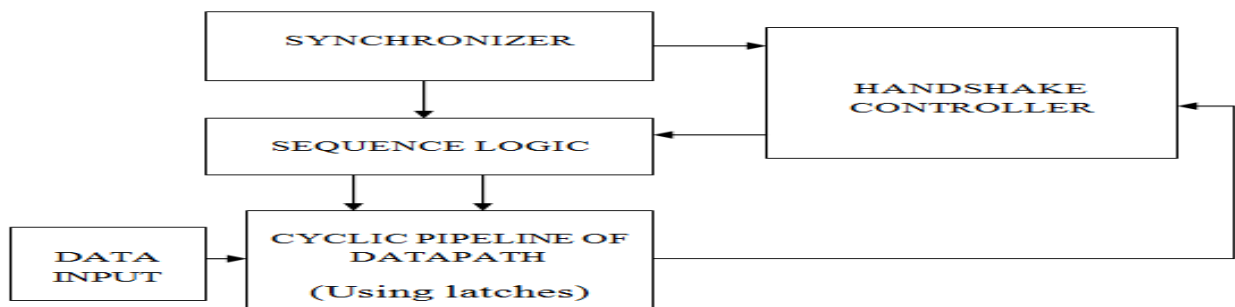
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## VLC 3029. ELIMINATING SYNCHRONIZATION LATENCY USING SEQUENCED LATCHING

### ARCHITECTURE DIAGRAM



**DESCRIPTION :** We Design a speculative method that hides synchronization latency by overlapping it with computation cycles. We verify the correctness of our approach through a field programmable gate array implementation and apply it to a number of synthesized benchmarks. Synthesis results reveal that our approach achieves average savings of 135% and 204% in area costs and nearly 100% in power costs compared to two similar speculative techniques. In the **MODIFICATION**, the sequencing of latches has been done by designing a control circuit which make the circuit work depend on the control inputs from the generator. The sequencing may be at the rising edge of clock or falling edge of the control clock, By doing this we can reduce lots of elements required for synchronizer and the control circuit may be done with a few Flip flops.

**DOMAIN :** Soft Error.

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2013



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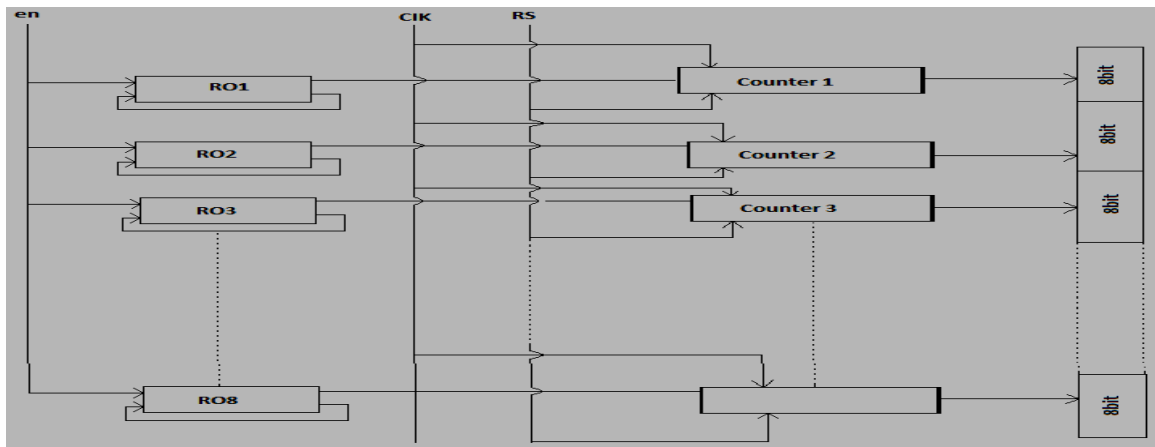
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## VLC 3030. GENERATION OF CHIP ID USING CONFIGURABLE RING OSCILLATOR

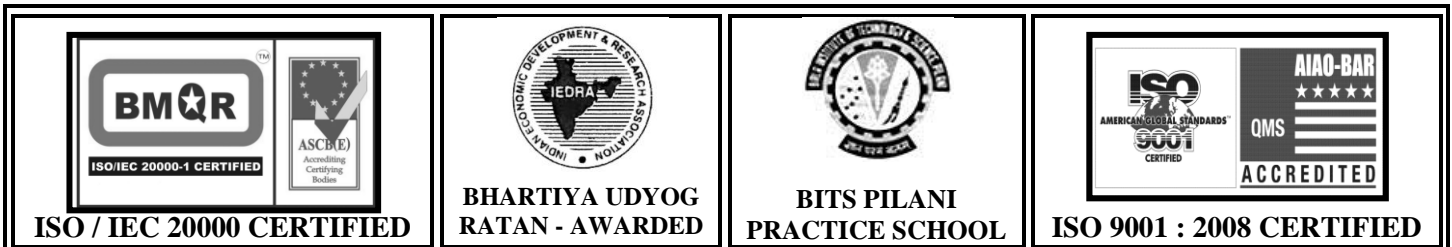
### ARCHITECTURE DIAGRAM



**DESCRIPTION :** In the **EXISTING SYSTEM**, there is no reconfigurable property. In the **PROPOSED SYSTEM**, chip id is generated with the help of ring oscillator, counter, register. Here ring oscillator is used to generate different frequency. Then the output of each ring oscillator feed into separate counter. Finally all the counter output's are put into single 64-bit register. This generated chip id have high inter-chip and intra-chip variation. In the **MODIFICATION**, we implement a BIST concept. The generated chip id's are stored into a RAM. And then we perform the all operation (write, read, compare) regards of BIST concept.

**DOMAIN :** Cryptography

**IEEE REFERENCE :** IEEE PAPERS on Digital System Design (DSD) 2013





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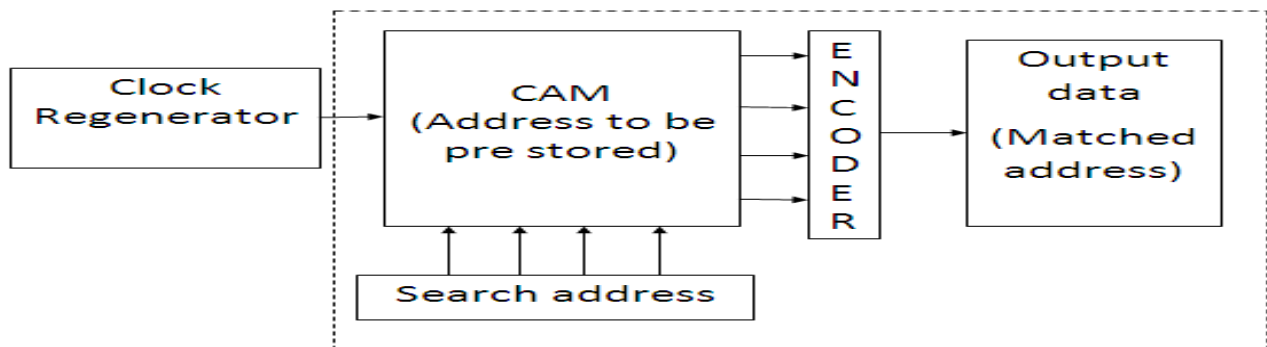
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## VLC 3031. A HIGH SPEED LOW POWER CAM WITH A PARITY BIT AND POWER-GATED ML SENSING

### ARCHITECTURE DIAGRAM



**DESCRIPTION:** In the **EXISTING SYSTEM**, the designed CAM require high power. In the **PROPOSED SYSTEM**, we design a CAM using cmos technology. Here first we design a cell using cmos. Then we form the memory matrix with the help of cmos cell. The output of the matrix feed into encoder block to specify the matched location. In the **MODIFICATION**, we implement the IP filtering concept. Here node allow the transaction only for authorized user. It means the authorized user id's are already stored in the CAM. So , unauthorized user id's are blocked by CAM.

**DOMAIN :** Memory Design.

**IEEE REFERENCE :** IEEE TRANSACTIONS on very large scale integration (VLSI) systems, 2013



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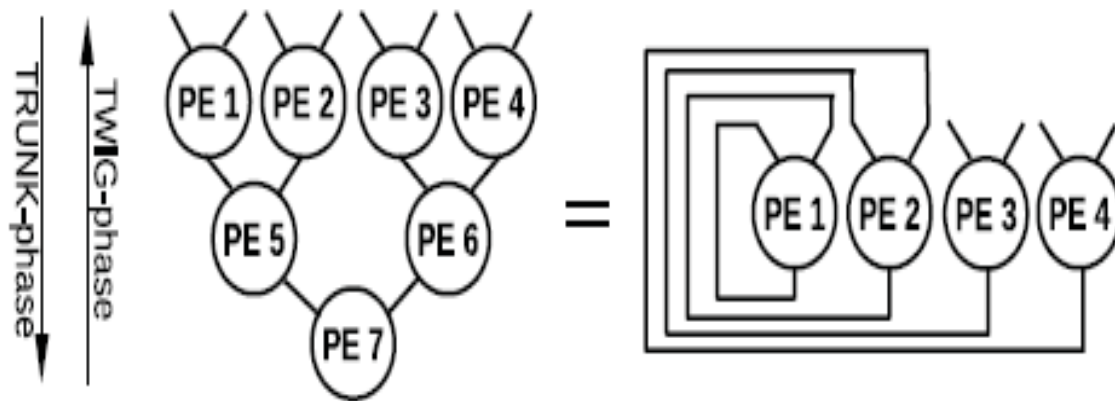
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## VLC 3032. LOW-POWER DIGITAL SIGNAL PROCESSOR ARCHITECTURE FOR WIRELESS SENSOR NODES

### ARCHITECTURE DIAGRAM



**DESCRIPTION:** In the **EXISTING SYSTEM**, need high power requirement. In the **PROPOSED SYSTEM**, we design the folded tree architecture. The use of folded tree method is to reduce the required processing element. If we reduce the processing element means the required power also reduced. In the **MODIFICATION**, we implement the NOC (Network On Chip) concept using VHDL. Here we use the file handling concept to perform NOC.

**DOMAIN :** NOC.

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2013



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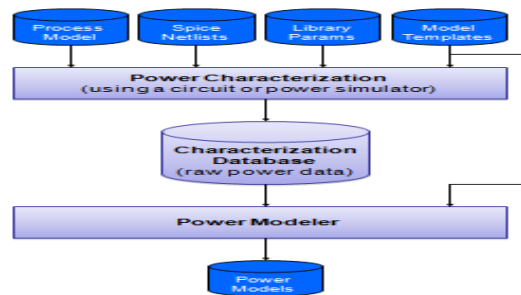
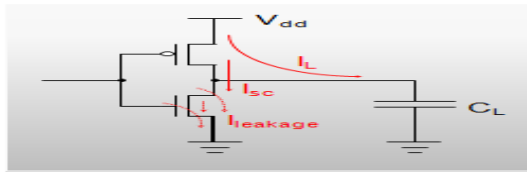
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## VLC 3033. EFFICIENT APPROACH FOR POWER REDUCTION BY USING MULTI-BIT FLIP-FLOPS

### ARCHITECTURE DIAGRAM



**DESCRIPTION:** In **EXISTING SYSTEM**, there is two inverter used. In the **PROPOSED SYSTEM**, to reduce the power consumption by replacing some flip flop with fewer Multi-Bit flip flops. We are using the Multi-Bit flip flops instead of more single bit flip flop in order to increase the clock synchronization. This will reduce the unnecessary power wastage through the use of multiple clock sinks. In the **MODIFICATION**, part we implement the Memory Device Using Gated Multi-Bit Flip Flop. Here the flip-flop replaced for power reduction in memory design. The procedure of flip-flop replacements is depending on the combination table. The memory designed by mainly using the Gated multi-bit flip flops. In this, power consumption of memory devices is reduced compare to the Multi-Bit flip flop memory.

**DOMAIN :** Low Power

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) Systems, 2013



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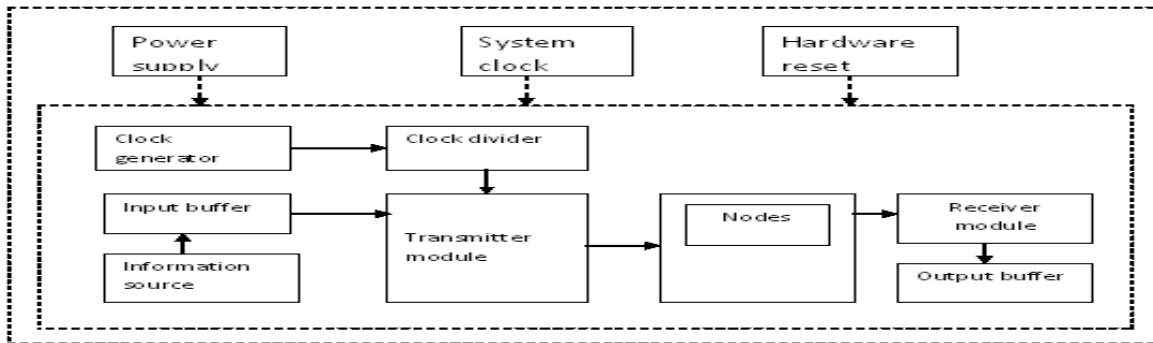
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## VLC 3034. SMART RELIABLE NETWORK-ON-CHIP

### ARCHITECTURE DIAGRAM







**DESCRIPTION:** In the **EXISTING SYSTEM**, not suitable for dynamic NOC. so, in the **PROPOSED SYSTEM**, we designed a online detection of data packet and adaptive routing algorithm errors. Both presented mechanisms are able to distinguish permanent and transient errors and localize accurately the position of the faulty blocks (data bus, input port, output port) in the NoC routers, while preserving the throughput, the network load, and the data packet latency. We provide localization capacity analysis of the presented mechanisms, NoC performance evaluations, and field-programmable gate array synthesis. In the **MODIFICATION**, part advanced routing algorithm is implemented where the data packets are sent in high speed and priority based approach. The advantage of doing this reduce the frequent checking of un connected nodes and making the return path delay.

**DOMAIN :** Network on Chip.

**IEEE REFERENCE :** IEEE TRANSACTIONS on Very Large Scale Integration (VLSI) systems, 2013

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